

PATENT
Serial No. 10/538,347
Amendment in Reply to Office Action of January 17, 2007

IN THE SPECIFICATION

Please amend the specification as follows:

Replace the paragraph spanning pages 5-6, between page 5, line 29, and page 6, line 13 of the specification with the following:

Figure 4 illustrates an example class AB type power amplifier 100 which may comprise either one of the stages shown in the exemplary circuit of Figure 3 and, is described in commonly-owned, co-pending U.S. patent application Ser. No. 10/189,233. For example, there is depicted an RF input 105, an output transistor 110 (e.g., Q1 or Q2) and a static bias current circuit 149 such that the bias current is going to be constant regardless of operating of temperature, variation of RF signal input, etc. The bias circuit 149 basically comprises a current mirror circuit including a transistor 120 that maintains a collector current that mirrors the collector current of the RF output transistor device. In effect, the quiescent current is determined by the current through the transistor 120. On a multistage amplifier this circuit can be used on any stage. The advantage is a temperature stable

PATENT

Serial No. 10/538,347

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bias current. The control loop allows the current to be monitored closely and I_{cq} can be minimized as much as possible. Further provided is a Vmode transistor 125 which is a transistor having a voltage ("V-mode") input 126 which operates under system control (not shown) to discretely modify the quiescent current between two different levels depending upon the V-mode voltage applied. This produces a power dissipation curve such as curve 24 shown in Figures 1 and 2.

Replace the paragraph on page 11, between lines 3-31 of the specification with the following:

Figure 10 is a diagram illustrating a circuit 300' according to a preferred embodiment of the invention that represents a portion of the output Class AB P.A. corresponding to the circuit portion 300 indicated in Figure 8. The circuit 300' illustrates the power (RF) input detector circuit 210, self-adaptable sliding circuit 250 and Q2 bias circuit according to the invention. The voltage output 215 of the detector circuit 210 is directly affected by the current passing through the detector and is fed into the self-adaptable slide circuit transistor 225 through resistor 227.

PATENT

Serial No. 10/538,347

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In operation, when the voltage 215 decreases (with an increase of power through the detector), the current through transistor 225 will decrease. In turn, the ratio between resistor 228 and transistor 120 is changed, as combination of the differential pair 325 holds the total current through all branches constant, the quiescent current through transistor 120, a mirror of Q2, is changed. Accordingly, the quiescent current I_{cq-2} through at the output transistor Q2 is automatically changed in the manner described herein, with changing RF input voltage. It should be understood that, in a preferred embodiment, the Vmode transistor 125 shown in ~~Figure 3~~ Figure 4 for discretely changing the quiescent current via a Vmode signal 126 may be additionally provided in parallel to the RF ~~detect~~ detector 210 and self-adaptable bias circuit 250 to provide the additional Vmode discrete quiescent current I_{cq-2} control. In this embodiment, there are two power ranges where the quiescent current I_{cq-2} through the output transistor Q2 changes: the self adapting sliding bias circuit will kick in at the higher power level (see (Figure 7(b)) and Vmode described in connection with Figure 4 will kick in at a predetermined threshold dictated by Vmode voltage 126, e.g., which

PATENT

Serial No. 10/538,347

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is used to lower the I_{cq} current at output power levels lower than a threshold power, e.g., 5 dBm, for example. The voltage at which the self-adapting bias circuit 250 kicks in, and the slope of change, are dependent upon the values of base resistor 227 and collector resistor 228 of the sliding bias circuit transistor 225 and a reference voltage 230 as shown in Figure 10. Those features are also dependant upon the values chosen for the detector, as it was described hereinabove. It should be understood that the circuit of Figure 10 has been modified to omit certain capacitor devices and other circuit elements that aid in the suppression of noise and enhance stability in the output stage circuits.